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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,356	04/20/2004	Richard Carl Phelps	0120-027	2594

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POTOMAC PATENT GROUP, PLLC  
P. O. BOX 270  
FREDERICKSBURG, VA 22404

EXAMINER

CLEARY, THOMAS J

ART UNIT PAPER NUMBER

2111

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/827,356	Applicant(s) PHELPS ET AL.	
	Examiner Thomas J. Cleary	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 03 November 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>20041103</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 4,419,724 to Branigin et al. ("Branigin") and US Patent Number 4,535,404 to Shenk ("Shenk").

3. In reference to Claim 1, Branigin discloses an apparatus for use in a computer system comprising: a bus architecture (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1), each module being assigned an ID (See Column 4 Lines 1-4); each module comprising: reception means for receiving and storing availability data indicative of the availability of modules (See Column 5 Lines 17-22); transaction request means for producing a transaction request including target address data indicating a destination ID for the transaction (See Column 8 Lines 23-29); decoding means for decoding the destination ID to produce an expected destination ID relating to a target module (See Column 8 Lines 27-29); comparison means for

analysing the stored availability data corresponding to the target module identified by the expected destination ID (See Column 8 Lines 29-40); and transaction means, responsive to the comparison means, for terminating the transaction request if the analysed availability data indicates that the target module is unavailable (See Column 8 Lines 29-40). Branigin teaches the use of device IDs as opposed to memory-mapped devices. Memory mapping devices is a well-known alternative to using device IDs. Branigin further does not teach the target module having an address range in the memory map which includes the target address data. Shenk teaches the use of memory-mapped devices (See Column 1 Lines 13-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the system of Branigin using the memory mapped devices of Shank instead of device ID's, resulting in the invention of Claim 1, because memory mapping devices is well known, allows communications with devices to be performed with normal memory reference instructions, and offers increased flexibility (See Column 1 Lines 25-28 and 51-52 of Shenk).

4. In reference to Claim 2, Branigin and Shenk teach the limitations as applied to Claim 1 above. Branigin further teaches a control means for controlling access to the bus architecture by the modules (See Figure 1 Number 100) and wherein the transaction means is further operable to forward, to the control means, a transaction request, if the analysed availability data indicates that the target module is available (See Column 8 Lines 33-40).

5. In reference to Claim 3, Branigin and Shenk teach the limitations as applied to Claim 1 above. Branigin further discloses a computer system comprising the apparatus (See Figure 1).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blum as applied to Claim 1 above, and further in view of US Patent Number 5,761,516 to Rostoker et al.

7. In reference to Claim 4, Branigin and Shenk teach the limitations as applied to Claim 1 above. Branigin and Shenk do not teach an integrated circuit comprising the apparatus. Rostoker teaches an integrated circuit having a plurality of devices, which can include processors, memory controllers, and I/O controllers (See Figure 2 and Column 2 Lines 10-16).

It would have been obvious to construct the device of Branigin and Shenk, on the integrated circuit of Rostoker, resulting in the invention of Claim 4, in order to provide a more cost-effective use of silicon real estate and provide much better price performance than conventional multichip designs (See Column 1 Line 65 – Column 2 Line 9 of Rostoker).

### ***Response to Arguments***

8. Applicant's arguments, see Pages 7-13, filed 3 November 2005, with respect to the rejection(s) of claim(s) 1-4 have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Branigin and Shenk.

### ***Conclusion***

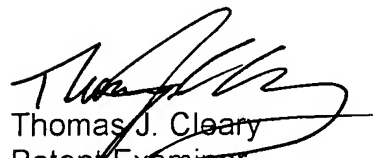
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

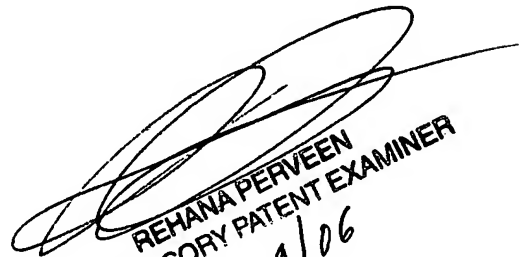
Art Unit: 2111

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC



Thomas J. Cleary  
Patent Examiner  
Art Unit 2111



REHANA PERVEEN  
SUPERVISORY PATENT EXAMINER  
11/19/06